

# 國立臺灣師範大學 99 學年度碩士班招生考試試題

科目：計算機系統

適用系所：資訊工程學系

注意：1.本試題共 5 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則不予計分。

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1. (3 分) Illustrate the structure of a process in memory.
2. (5 分) Illustrate the diagram of process state and explain each state transition in detail.
3. (5 分) Illustrate how the operating system can schedule the process in round-robin scheduling with different time quanta. Note that we assume that there is a timer in the machine.
4. (7 分) (a) What are the necessary conditions for a deadlock to arise? (b) By ensuring that at least one of these conditions cannot hold, we can prevent the occurrence of a deadlock. Please show a scheme to ensure that the circular-wait condition never occurs in the system. (c) In terms of deadlock avoidance, why may an unsafe state not lead the system to the deadlock?
5. (5 分) (a) What are the differences between multiprogramming and multi-tasking systems? (b) Since the operating system and the user processes share the resources of the computer system, we need to make sure that an error in a user process does not influence the execution of other processes. For example, if a process gets stuck in an infinite loop, this loop could prevent the operation of many other processes. Can the multiprogramming and multi-tasking systems solve the above problem?
6. (5 分) Give the reason why a system using paging does not have the external fragmentation. Assume a computer is with 2GB of main memory. The size of a frame is 4KB. In case there are 1000 processes executed in it, how much memory is wasted in average in term of the internal fragmentation.

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7. (5 分) The Unix file system (UFS) is a file system used by many Unix and Unix-like operating systems. Show the structure of the UNIX inode.
8. (3 分) Can we invoke system calls in high-level programming languages *directly* without using the assembly language? Please also give the reason.
9. (5 分) Typically, the operating system uses two levels of internal tables for file operations: a per-process open file table and a system-wide open file table. Where are the file pointer and the memory cache of the file stored? Please also show the reason why the other table is inappropriate.
10. (7 分) The signal is one of the mechanisms for the interprocess communication in Unix operating system. What are the differences between the signal and message? What are the related system calls for signal? How does the Unix operating system implement the signal?

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11.(14 分) The following tables list some examples of MIPS machine language formats and its register conventions.

Name	format	example						Comments
Add	R	0	18	19	17	0	32	add \$s1,\$s2,\$s3
Sub	R	0	18	19	17	0	34	sub \$s1,\$s2,\$s3
Addi	I	8	18	17	100			addi \$s1,\$s2,100
Lw	I	35	18	17	100			lw \$s1,100(\$s2)
Sw	I	43	18	17	100			sw \$s1,100(\$s2)
Beq	I	4	17	18	25			beq \$s1,\$s2,100
Bne	I	5	17	18	25			bne \$s1,\$s2,100
Slt	R	0	18	19	17	0	42	slt \$s1,\$s2,\$s3
J	J	2	2500					j 10000
Jr	R	0	31	0	0	0	8	jr \$ra
Jal	J	3	2500					jal 10000
Field size		6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions 32 bits
R format	R	op	rs	rt	rd	shamt	funct	Arithmetic instruction
I format	I	op	rs	rt	Address/immediate			Data transfer, branch, and immediate

Name	Register number
\$zero	0
\$v0-\$v1	2-3
\$a0-\$a3	4-7
\$t0-\$t7	8-15
\$s0-\$s7	16-23
\$t8-\$t9	24-25
\$gp	28
\$sp	29
\$fp	30
\$ra	31

In the memory of a MIPS computer, the contents of locations 80000H to 80007H are listed as follows.

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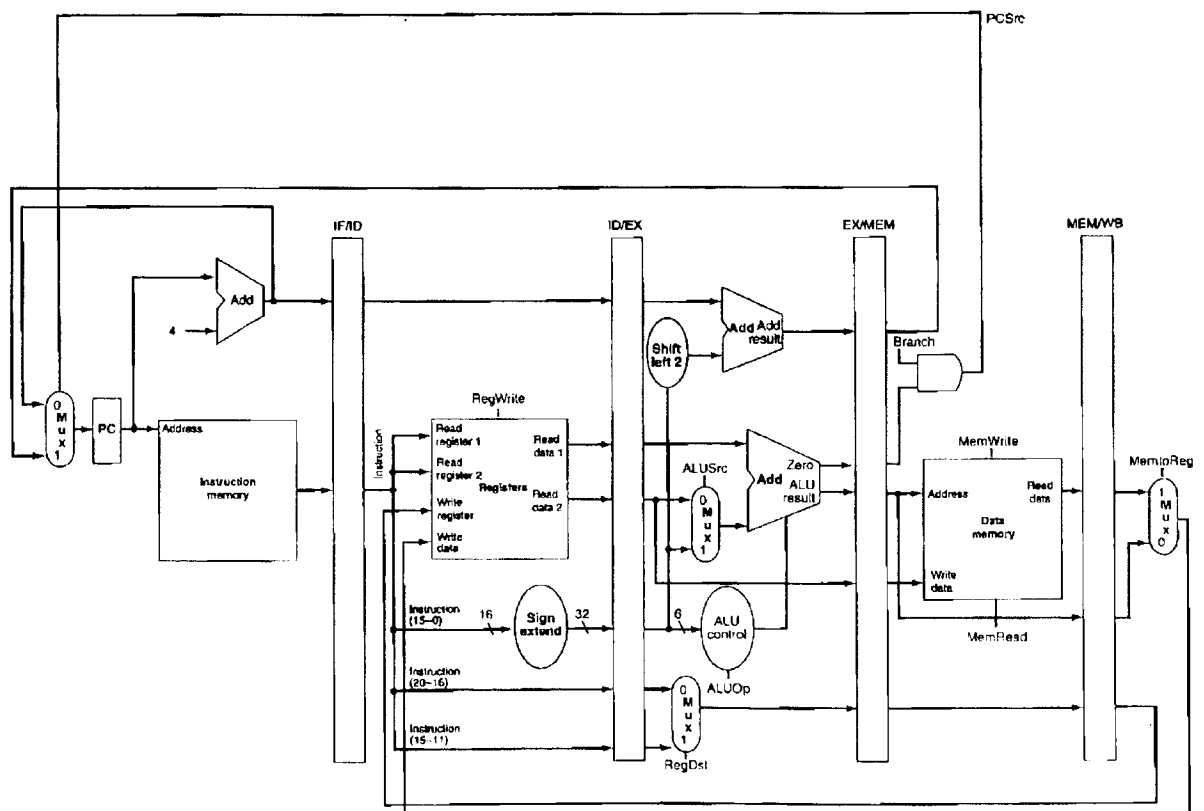
Address	content
80000H	02H
80001H	49H
80002H	40H
80003H	20H
80004H	ADH
80005H	52H
80006H	00H
80007H	C8H

What are the assembly codes that represent the machine codes stored in these locations?

12.(14 分) The following instruction sequence is executed in the pipelined datapath shown below.

```

sw    $t1,0($s2)
lw    $t2,4($s2)
add   $t3,$t1,$t2
sub   $t4,$t1,$t2
sub   $t5,$t2,$t1
and   $t6,$t1,$t2
    
```



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The input and output relations of the ALU control logic are listed in the following table.

Instruction	ALUop	ALU control input
lw	00	0010
sw	00	0010
add	10	0010
sub	10	0110
and	10	0000

At the beginning of the 1<sup>st</sup> clock cycle, the *sw* instruction is fetched by the datapath. Assume the datapath has a forwarding unit and a hazard detection unit. At the 5<sup>th</sup> clock cycle, (1) what is the instruction operated in each of the pipeline stages? And (2) what is the value on each of all the control signals (RegWrite, RegDst, ...)?

13.(10 分) Consider a computer operates with clock frequency 2GHz. It has the split cache organization. If all memory accesses are hit in the cache, the CPI is 2. The cache miss penalty is 40ns. Suppose a program is run on this computer. Among the instructions been executed, 25% of them are memory access instructions. The miss rate for instruction cache is 2%, and for data cache is 4%. What is the actual CPI?

14.(12 分) Consider a computer has a fully associative mapped 32 bytes cache with block size of 8 bytes. The replacement policy is LRU. A program is run on this machine. The memory access sequence in word address is 0, 1, 2, 5, 6, 7, 3, 1, 2, 3, 4, 5, 6, 7, 20, 21, 22, 23, 0, and 1. What is the cache hit rate for this program fragment?