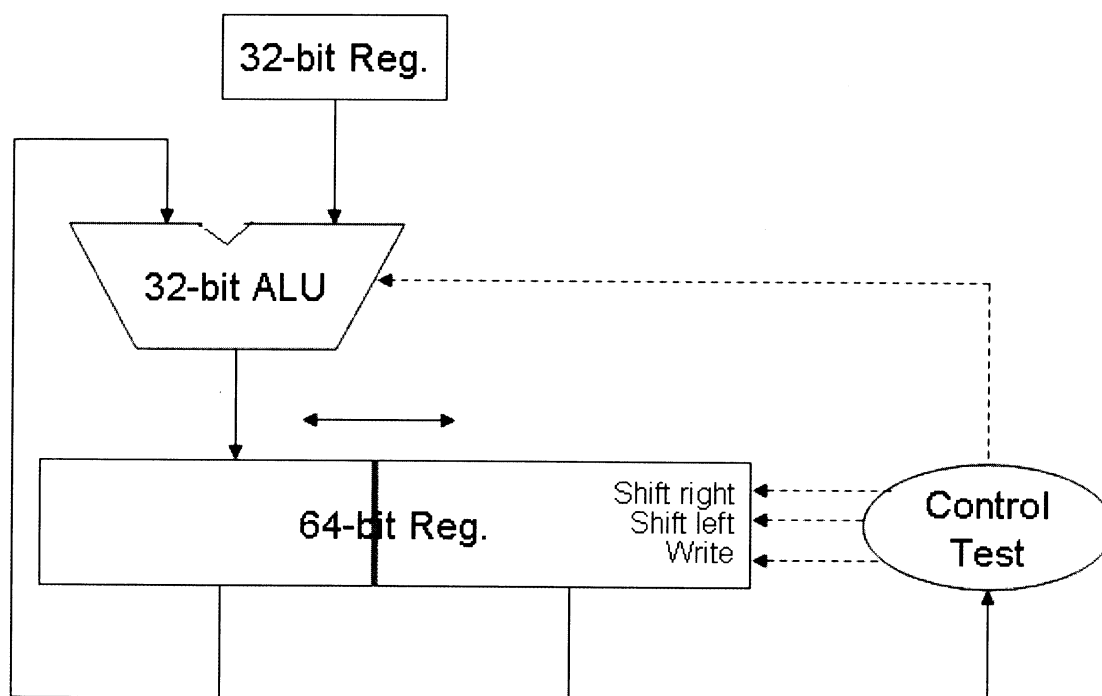


國立臺灣師範大學九十七學年度碩士班考試入學招生試題

計算機系統 科試題 (資訊工程學系用 , 本試題共 4 頁)

注意： 1. 依次序作答，只要標明題號，不必抄題。
2. 答案必須寫在答案卷上，否則不予計分。

1. Explain how the following hardware can perform both 32-bit multiplications and divisions. (13 分)



2. Explain how the following techniques can be used to increase the performance of a pipelined processor?

- (a) forwarding, (3 分)
- (b) delayed branch, (3 分)
- (c) reservation station, (3 分)
- (d) superscalar processor, (3 分)
- (e) loop unrolling. (3 分)

3. Consider an instruction set is implemented with the multi-cycle architecture.

The instructions are classified into 4 classes, i.e. calculation, branch, memory read, and memory write. The stages of instruction execution and the execution times of each stage are shown in the following table:

| | Instruction fetch | Decode and fetch operands | ALU | Memory read/write | Write back |
|----------------|-------------------|---------------------------|------|-------------------|------------|
| Calculation | V | V | V | | V |
| Branch | V | V | V | | |
| Memory read | V | V | V | V | V |
| Memory write | V | V | V | V | |
| Execution time | 60ns | 25ns | 40ns | 60ns | 25ns |

Consider a program executing on this machine. The distribution of instructions is shown below.

| Calculation | Branch | Memory read | Memory write |
|-------------|--------|-------------|--------------|
| 47% | 20% | 21% | 12% |

Calculate the average execution time for an instruction. (10 分)

4. Consider a computer has clock rate of 2.5GHz. The CPI with a perfect cache is 3. The cache miss penalty is 40ns. Assume the cache miss rate is 6%.
- (a) What is the actual CPI? (6 分)
 - (b) If a second level cache with the 1st level miss penalty 10ns is added, the miss rate to the main memory is reduced to 2%. What is the speedup? (6 分)
5. When you adopt priority scheduling, some processes may never get the CPU, which is known as starvation. What is the technique used in modern OS to prevent such starvation? i.e., please propose a method that eventually grants CPU to the low-priority processes. (5 分)
6. There are many kinds of process/thread synchronization provided by modern O.S., such as semaphores, critical sections, monitor, mutex, and message queues.
- Please answer if the following statements are true or false:
- (a) Monitor is more powerful and expressive than semaphores. (1 分)
 - (b) Critical section can be implemented by semaphores, message queues, but not monitor. (1 分)
 - (c) Semaphores can be implemented by critical sections with shared variables. (1 分)
 - (d) Critical section can be supported by spinlock. (1 分)
 - (e) Monitor is considered difficult to use than semaphore. (1 分)
 - (f) Message queue can not be implemented by semaphore and monitor. (1 分)
 - (g) The semantics of semaphore's *wait(S)* and monitor's *S.wait()* are equivalent. (1 分)
 - (h) A message queue with size of 1 is equal to semaphore with value initialized to 0. (1 分)
 - (i) Critical sections, mutex, and semaphore are executed with same performance under Windows. (1 分)
 - (j) All these synchronization methods cause mode switch to kernel mode. (1 分)
7. A partition is formatted into FAT 32. The disk block is 4K bytes in size. What is maximum size this partition can be? (5 分)

8. A memory system has 3 frames. It adopts second chance (clock) algorithm for page allocation. Consider the following page reference string

1, 2, 3, 4, 2, 3, 5, 1, 3, 2

In the last page reference, a frame containing page reference X is replaced by the page reference 2. What is X? (10 分)

9. Consider a system with the following properties:

- A 64K byte logical address space,
- A physical memory of 16K bytes,
- A simple (one-level) page table address translation implementation using page size of 4096 byte,
- The page tables are stored in physical memory,
- The access time of physical memory is 100μs.

(a) How many bits wide is a logical address? (2 分)

(b) What is the minimum number of bits a pointer in a C program compiled for this machine would need to occupy? (2 分)

(c) Assuming it also needs to hold a valid-bit, a referenced-bit and a modified-bit, what is the **minimum** number of bits wide a page table entry (PTE) needs to be? (2 分)

(d) Assuming each page table entry is actually 16 bits wide, how many bytes would a page table of a process occupy in a physical memory? (2 分)

(e) How many page table entries would be needed if this system is implemented by inverted page table? (2 分)

10. Multi-level paging system is in general slower than one-level paging but modern hardware still adopts it for practical reasons. What kind of advantages can we get from a multi-level paging system in terms of:

(a) kernel memory management and allocation, (4 分)

(b) user program memory segment layout (such as stack and heap allocation), (3 分)

(c) memory saving in page table allocation. (3 分)

i.e., please explain how multi-level paging improves in these aspects.