國立臺灣師範大學九十六學年度碩士班考試入學招生試題

計算機系統 科試題（資訊工程學系用，本試題共 6 頁）

注意：1.依次序作答，只要標明題號，不必抄題。
2.答案必須寫在答案卷上，否則不予計分。

1. Consider a cache with 2K blocks and a block size of 16 bytes. Suppose the address is 32 bits.

   (a) Suppose the cache is direct-mapped. Find the number of sets in the cache. Compute the number of tag bits *per cache block*. (5 分)

   (b) Repeat part (a) when the cache becomes a 2-way set associative cache. (5 分)

   (c) Repeat part (a) when the cache becomes a fully associative cache. (5 分)

2. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 500 ps, and computer B has a clock rate of 2.5 GHz. Consider a program having 1000 instructions.

   (a) Suppose computer A has a clock cycles per instruction (CPI) 2.3 for the program. Find the CPU time (in ns) for the computer A. (5 分)

   (b) Suppose the CPU time of the computer B is 800 ns for the same program. Compute the CPI of computer B for the program. (5 分)

3. Assume a MIPS processor executes a program having 800 instructions. The frequency of loads and stores in the program is 25%. Moreover, an instruction cache miss rate for the program is 1%, and a data cache miss rate is 4%. The miss penalty is 100 cycles for all misses.

   (a) Find the total number of instruction miss cycles. (5 分)

   (b) Find the total number of data miss cycles. (5 分)

4. Consider a 5-stage (IF, ID, EX, MEM, WB) MIPS pipeline processor with hazard detection unit. Suppose the processor has instruction memory for IF stage, and data memory for MEM stage so that the structural hazard for memory references can be avoided.

(a) Assume *no forwarding unit* is employed for the pipeline. We are given a code sequence shown below.

```
LD    R1, 10(R2);      R1 ← MEM[R2+10]
SUB   R4, R1, R6;      R4 ← R1-R6
ADD   R5, R1, R6;      R5 ← R1+R6
```

Show the *timing of each instruction* of the code sequence. Your answer may be in the following form. (5 分)

Instruction		Clock Cycle									
		1	2	3	4	5	6	7	8	9	10
LD	R1, 10(R2)	IF	ID	EX	MEM	WB					
SUB	R4,R1,R6										
ADD	R5,R1,R6										

(b) Repeat part (a) when a forwarding unit is used. (5 分)

(c) Consider another code sequence shown below.

```
SUB   R1, R3, R8;      R1 ← R3-R8
SUB   R4, R1, R6;      R4 ← R1-R6
ADD   R5, R1, R6;      R5 ← R1+R6
```

Suppose both hazard detector and forwarding unit are employed. Show the timing of each instruction of the code sequence. (5 分)

5. (a) What are the differences between a trap and an interrupt? (2 分)

(b) Can traps be generated intentionally by a user program? If so, for what purpose? (2 分)

6. In terms of dual-mode operation, answer the following questions:

(a) Why do most of the processors support this mechanism? (2 分)

(b) When does the hardware switch from user mode to kernel mode? (2 分)

(c) What is the relationship between system calls and dual-mode operation? (2 分)

7. (a) What are the requirements that a correct solution to the critical section problem must satisfy? (2 分)

(b) Consider the following code fragments. Prove that one of the requirements is not satisfied. Note that `TestAndSet(&lock)` is executed atomically. (3 分)

```
Do {
    while ( TestAndSet(&lock) );
    //critical section
    lock=FALSE;
    // remainder section
} while(TRUE);
```

8. In case that there exists a cycle in a resource-allocation graph, does the deadlock situation always occur? (Yes/No) (2 分)

9. Describe three general methods for passing parameters to the operating system. (3 分)

10. Which of the following components of program state are shared across threads in a multithreaded process? (2 分)

i. Register values

ii. Heap memory

iii. Global variables

iv. Stack memory

11. What are the differences between the system call, library call, and subroutine call? (4 分)

12. (a) Illustrate the structure of a process in memory. Note that the operating system should support the execution of contemporary programming languages such as C++ in which recursive function and heap memory allocation must be supported. (3 分、請畫圖說明)

(b) The multi-level paging system suffers from memory access overhead. Show the reason why most contemporary CPUs support it. (3 分)

13. (a) What is the purpose of the translation look-aside buffer (TLB)? (2 分)

(b) What is the relation between the TLB and processor affinity? (2 分)

(c) Generally speaking, every time a new page table is selected (for instance, with each context switch), the TLB must be flushed to ensure that the next executing process does not use the wrong translation information. How can we avoid the overhead of flushing the TLB? (2 分)

14. (a) What is the copy-on-write technique? (2 分)

(b) How does the operating system and CPU implement the copy-on-write? (2 分)

15. Typically, the operating system uses two levels of internal tables: a per-process open file table and a system-wide open file table for handling the file operations. For the following data items, which are stored in the system-wide open file table? (3 分)

i. File pointer which is used to track the last read-write location as a current-file-position pointer.

ii. File-open count

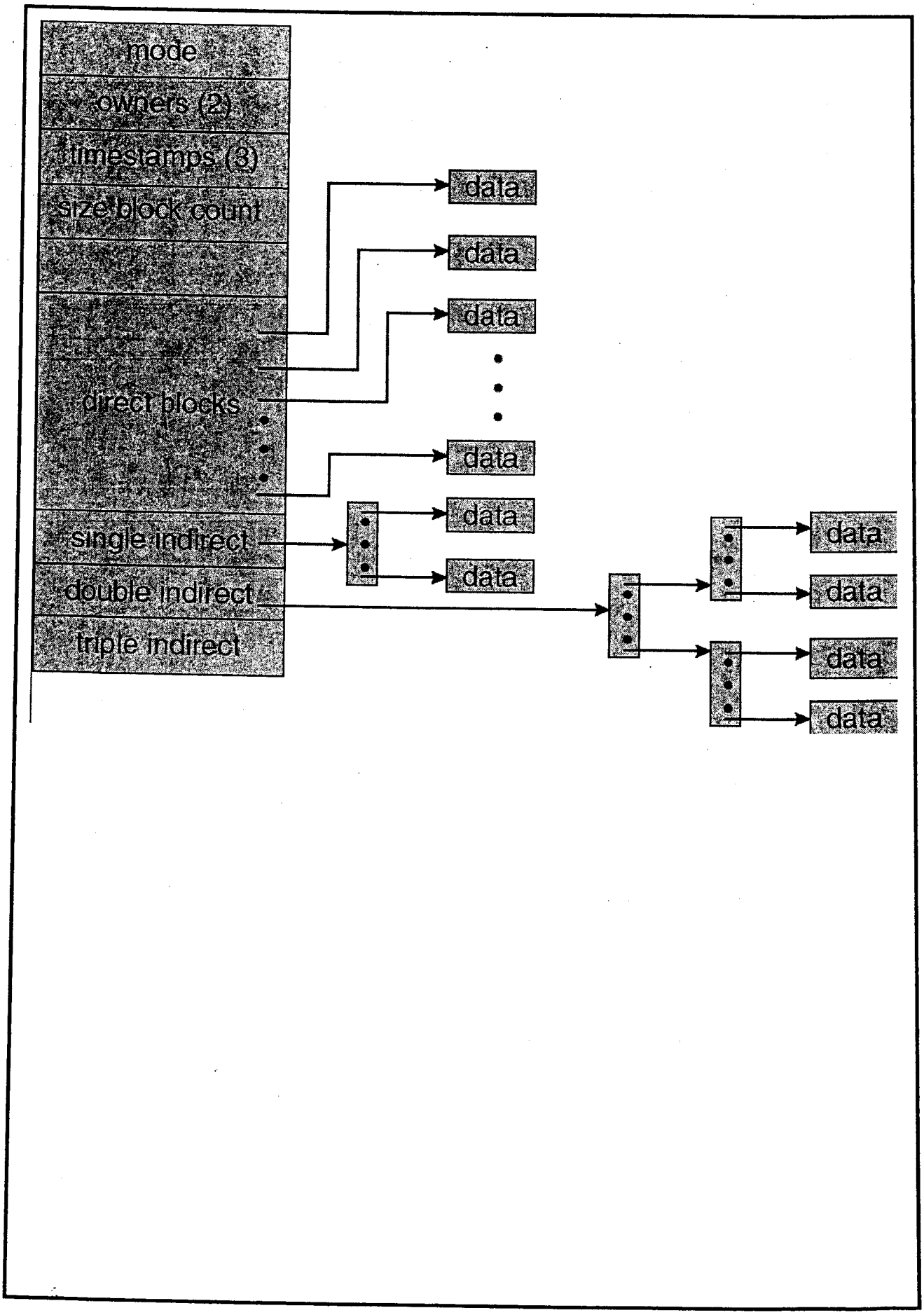
iii. Disk location of the file

iv. Access rights during the open session

v. Access permission of the file

vi. Memory Cache of the file

16. The allocation method of the UFS is a combination of the linked scheme and the multilevel index as shown in the following figure. It keeps the first, say, 15 pointers of the index block in the file's inode. The first 12 of these pointers point to direct block; that is, they contain addresses of blocks that contain data of the file. Assume that each pointer is four-byte long and the block size is 4KB. What is the maximal size of the file if only direct blocks are used? What is the maximal size of the file if the "single indirect" pointer is used? (5 分)


mode
owners (2)
timestamps (3)
size block count
direct blocks
single indirect
double indirect
triple indirect
data
data
data
data
data
data
data
data
data